A Control Method for Full Voltage Conversion Ratio for a Zero-Inductor-Voltage Converter

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***Abstract*— In this paper, a new gate drive control strategy for the 7-Switch Zero-Inductor-Voltage (ZIV) converter is proposed. The converter conventionally has a fixed input-to-output voltage conversion ratio. It has almost zero output current ripple that has led to high power density and high efficiency at high output current. However, the fixed conversion ratio has limited the converter's application. Nonetheless, with the new gate drive control strategy, the control ability of the converter is significantly extended while maintaining a very small inductor value. Unlike the other control methods introduced in the literature, this method does not need any auxiliary components, and the regulation range is from zero to unity. At the same time, the output current ripple is kept low to achieve high efficiency and high power density. In this paper, the performance of the proposed control method has been analyzed and validated by a 250W prototype, 20-60V input voltage, 12V/21A output, with average efficiency over the full line (20 to 60V) and load (25% to 100%) of 97.54%.**

Keywords*— Full voltage conversion range, high efficiency, switched capacitor converter, zero-inductor-voltage.

I. Introduction

The switched-capacitor converters (SCCs) are being widely used such as data center applications. The conventional SSCs were only composed of switches and capacitors that made them suffer from high current spikes due to paralleling capacitors with uneven voltage level which is known as charge redistribution loss [1]. This has caused power loss known as charge redistribution loss. Also, a major limitation of these converters is that the voltage conversion ratio is fixed [1-2], which hinders these converters from being utilized in most applications. To eliminate these issues, inductors are inserted in series with the capacitors and form some resonant tank in the converter. This new generation of the SCCs such as Switched Tank Converters (STC) [3-6]. These kinds of SSCs can provide soft switching for the switches. There is another type of resonant SCC with an integrated inductor which is called Resonant Switched Capacitor Converters (RSCCs) [2, 7-9]. The other type of popular switched capacitor converter is Zero-Inductor Voltage (ZIV) converters [10-12]. The same as RSSCs, ZIVs have an integrated inductor, however, the flying capacitor value is much larger. Therefore, the resonant frequency drops far below switching frequency. Although the converter does not operate in resonant mode, the voltage variation across the flying capacitors becomes very small, in which by adopting a proper gate drive control strategy, the voltage across the inductor, in every interval during a switching cycle, becomes zero. This advantage makes the inductor's current ripple almost zero, leading to lower RMS current. Since the SSCs are mainly being used in low voltage, high current applications, the conduction loss forms a big portion of total power loss in these converters, low RMS current effectively improves efficiency.

However, the voltage regulation is still a major disadvantage in these converters. Nevertheless, in some studies, they achieved a limited range of voltage regulations [4-10, 13]. Usually, STCs use phase shift technics, and some other control duty cycle [9] to regulate the voltage, that in some cases they need to sense inductor's voltage [9]. These techniques sacrifice efficiency, and the voltage conversion range is very narrow [4-5]. Some of the RSCCs use frequency modulations to adjust output voltage [6-8], but when the conversion range widens, efficiency drops dramatically. The other solution is to connect a buck converter in series with a SCC converter [13-14]. However, since it is a lossy converter and has to deliver the nominal output current, the overall efficiency of these converters is low.

In this paper, a new pulse arrangement is going to be presented to extend the voltage conversion ratio of the 7-switch ZIV converter to the fullest. The converter is shown in Fig. 1, which was introduced in [10]. In this paper, a new control method is going to be discussed for this converter. This new control method does not need any further component to be added to the converter. It only uses the duty cycle to regulate the output voltage. Moreover, this new method keeps the inductor current as low as possible which is the key point in SCCs to achieve very high efficiency.

II. Converter Operation Principle

According to Fig.1, the converter is comprised of two stages and an output filter. The first stage includes four switches (S_1,

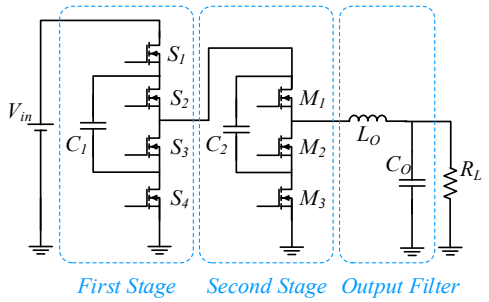


Fig. 1 The 7-Switch ZIV converter circuit [10]

S_2, S_3, and S_4), and a flying capacitor C_1. The second stage is formed by three switches (M_1, M_2, and M_3) and a flying capacitor C_2. Moreover, inductor L_O and capacitor C_O shape the output filter. In this figure, the input source and output load symbols are V_{in} and R_L, respectively. Based on the duty cycle of switch S_1 (D) value, the converter's operation is divided into four modes as follows:

Mode I: $0 \le D \le 1/4$
Mode II: $1/4 < D \le 1/3$
Mode III: $1/3 < D \le 1/2$
Mode IV: $1/2 < D \le 1$

The converter operation in these four modes will be discussed in detail.

A. MODE I: $0 \le D \le 1/4$

The pulse pattern and inductor's current in a switching cycle for the $0 \le D \le 1/4$, and the current flow in each interval, are presented in Fig.2. Therefore, one switching cycle could be divided into six intervals that are explained in detail below.

Interval 11 [t_{10} t_{11}]: At t_{10}, S_1 and S_3 turn on. Since M_2 was turned on before, the voltage across the inductor L_O becomes V_{in}-V_{C1}-V_{C2}-V_O. So, the inductor's current variation can be calculated as:

$$\Delta i_{Lo\_11} = \frac{DT_s}{L_o}(V_{in} - V_{C1} - V_{C2} - V_O) \quad (1)$$

where V_{C1}, V_{C2}, and V_O are voltage for first and second flying capacitor and output voltage, respectively. Also, T_S is the switching period. This current, charges both capacitors C_1 and C_2. Interval 11 ends at t_{11}, when S_1 and S_3 go off.

Interval 12 [t_{11} t_{12}]: At t_{11}, S_1 and S_3 go off and only M_2 remains on until t_{12}. In this interval, the inductor's current flows through M_2 and the body diode of M_3. As a result, the voltage across the inductor becomes -V_O, and the current variation is:

$$\Delta i_{Lo\_12} = \frac{(0.25-D)T_s}{L_o}(-V_O) \quad (2)$$

This interval finishes at t_{12}, when S_2 and S_4 turn on.

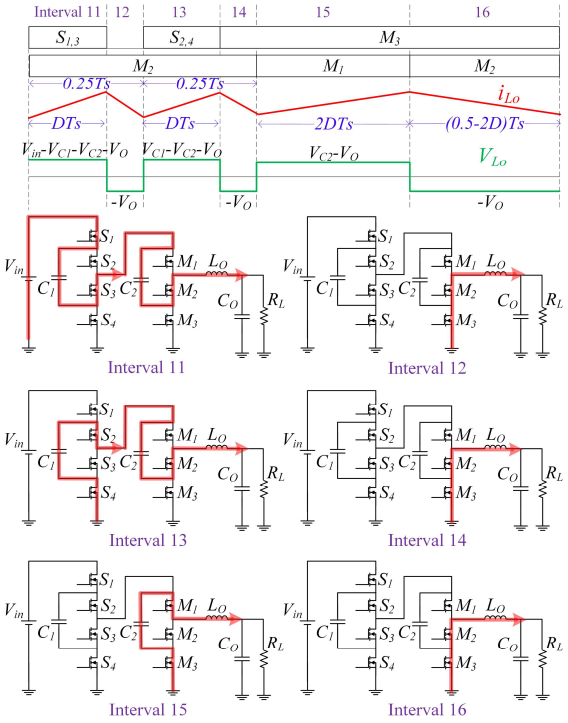


Fig. 2 Pulse arrangement, inductor current and voltage, and converter's equivalent circuit in Mode I.

Interval 13 [t_{12} t_{13}]: At t_{12}, S_2 and S_4 turn on and M_2 is still on. So, in this interval, the voltage across the inductor is equal to V_{C1} -V_{C2} -V_O, and the inductor's current change is:

$$\Delta i_{Lo\_13} = \frac{DT_s}{L_o}(V_{C1} - V_{C2} - V_O) \quad (3)$$

This current discharges C_1 and charges C_2. The interval ends at t_{13}, when S_2 and S_3 turn off.

Interval 14 [t_{13} t_{14}]: At t_{13}, S_2 and S_4 are turned off and M_3 turns on. Also, M_2 remains on. Therefore, the inductor's current flows through M_3 and M_2 leading to -V_O across the inductor. So, its current variation is:

$$\Delta i_{Lo\_14} = \frac{(0.25-D)T_s}{L_o}(-V_O) \quad (4)$$

This interval finishes at t_{14}, when M_2 and M_1 toggle their condition.

Interval 15 [t_{14} t_{15}]: At t_{14}, M_2 goes off and M_1 turns on. So, the voltage across the inductor becomes V_{C2}-V_O leading to the current variation equal to:

$$\Delta i_{Lo\_15} = \frac{2DT_s}{L_o}(V_{C2} - V_O) \quad (5)$$

This current discharges C_2. The interval ends at t_{15}, when M_1 turns off and M_2 turns on again.

Interval 16 [t_{15} t_{16}]: At t_{15}, M_1 turns off and the same as the fourth interval only M_2 and M_3 are on. So, the voltage across the inductor is equal to $-V_O$ and the current variation is:

$$\Delta i_{Lo\_16} = \frac{(0.5-2D)T_S}{L_o}(-V_O) \quad (6)$$

The interval ends at t_{16}=Ts, when M_3 turns off and S_1 and S_3 turn on again.

When the duty cycle is zero, the converter is off, and when it increases from zero to *1/4*, the converter's operation is the same as the six intervals explained above. As D approaches *1/4* intervals 2, 3, and 6 shrink, and whenever it becomes equal to 1/4, these intervals totally vanish. At this condition, the voltage across the inductor is zero in all intervals, as a result the current ripple will be zero. When the duty cycle keeps increasing and passes 1/4, the converter's operation enters Mode II.

B. MODE II: 1/4<D≤1/3

The pulse pattern and inductor's current in a switching cycle for the *1/4<D≤1/3,* and the current flow in each interval, are presented in Fig. 3. Therefore, one switching cycle could be divided into four intervals that are explained in detail below.

Interval 21 [t_{20} t_{21}]: At t_{20}, S_1 and S_3 turn on and M_1 is already on from the previous switching cycle, the voltage across the inductor L_O is equal to V_{in}-V_{C1}-V_O. Hence, the inductor's current variation can be calculated as:

$$\Delta i_{Lo\_21} = \frac{(4D-1)T_S}{L_o}(V_{in} - V_{C1} - V_O) \quad (7)$$

This current, charges the first flying capacitor C_1. This interval ends at t_{21}, when S_1 and S_2 go off.

Interval 22 [t_{21} t_{22}]: At t_{21}, M_1 goes off and M_2 turns on. Until t_2, S_1, S_3 and M_2 stay on. In this interval, the inductor's current flows through C_1 and C_2 charging both capacitors.

Therefore, the voltage across the inductor becomes V_{in}-V_{C1}-V_{C2}-V_O, and the current variation is:

$$\Delta i_{Lo\_22} = \frac{(1-3D)T_S}{L_o}(V_{in} - V_{C1} - V_{C2} - V_O) \quad (8)$$

This interval finishes at t_{22}, when S_2 and S_4 turn on.

Interval 23 [t_{22} t_{23}]: At t_{22}, S_2 and S_4 turn on and M_2 is still on. So, in this interval, the voltage across the inductor is equal to V_{C1}-V_{C2}-V_O, and the inductor's current change is:

$$\Delta i_{Lo\_23} = \frac{DT_S}{L_o}(V_{C1} - V_{C2} - V_O) \quad (9)$$

This current discharges C_1 and charges C_2. This interval ends at t_{23}, when S_2 and S_3 turn off.

Interval 24 [t_{23} t_{24}]: At t_{23}, S_2, S_4 and M_2 turn off. At the same time M_1 and M_3 turn on. As a result, C_2 discharges and the

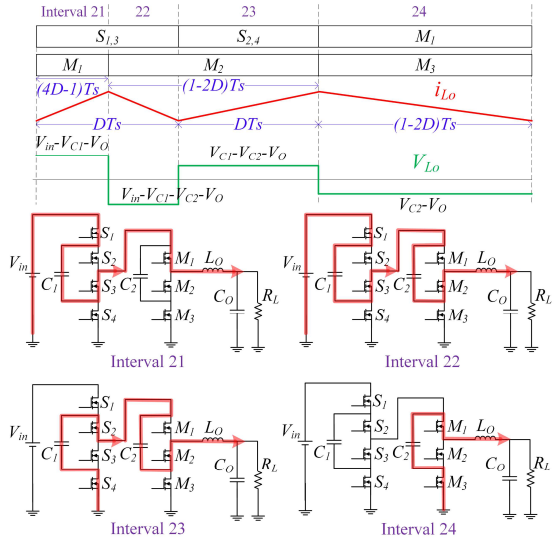


Fig. 3 Pulse arrangement, inductor current and voltage, and converter's equivalent circuit in Mode II.

inductor's current flows through M_1 and M_3 leading to V_{C2}-V_O across the inductor. Therefore, its current variation is:

$$\Delta i_{Lo\_24} = \frac{(1-2D)T_S}{L_o}(V_{C2} - V_O) \quad (10)$$

This interval finishes at Ts, when M_3 turns off but M_1 stays on.

When the duty cycle is greater than 1/4 and less than 1/3 the converter operates in the four intervals shown in Fig. 3. As the duty cycle increases, interval 2 shortens. However, when *D=1/3*, this interval completely vanishes. At this condition, the voltage across the inductor is zero in all intervals, as a result the current ripple will be zero. As the duty cycle continues to increase beyond 1/3 the converter enters Mode III.

C. MODE III: 1/3<D≤1/2

The pulse pattern and inductor's current in a switching cycle for the *1/3≤D≤1/2,* and the current flow in each interval, are presented in Fig. 4. Therefore, one switching cycle could be divided into four intervals that are explained in detail.

Interval 31 [t_{30} t_{31}]: At t_{30}, S_1 and S_3 turn on. Since M_1 is already on from the previous switching cycle, the voltage across the inductor L_O is V_{in}-V_{C1}-V_O. So, the inductor's current variation can be calculated as:

$$\Delta i_{Lo\_31} = \frac{DT_S}{L_o}(V_{in} - V_{C1} - V_O) \quad (11)$$

This current, charges the flying capacitor C_1. This interval ends at t_{31}, when S_1 and S_2 go off.

Interval 32 [t_{31} t_{32}]: At t_{31}, S_1, S_3 and M_1 go off and S_2, S_4 and M_2 turn on. Until t_2, M_2 stays on. In this interval, the inductor's current flows through both flying capacitors

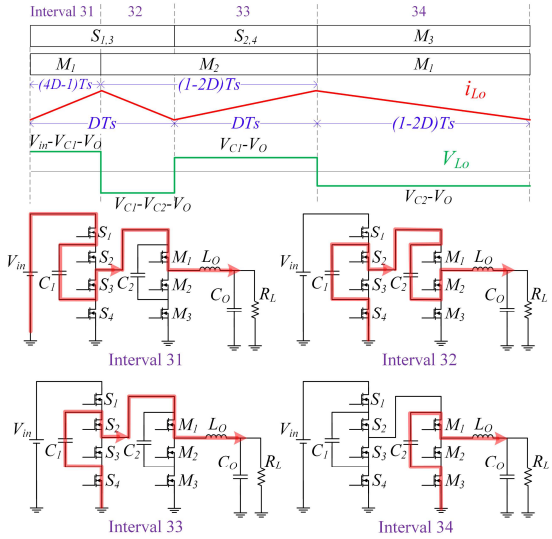


Fig. 4 Pulse arrangement, inductor current and voltage, and converter's equivalent circuit in Mode III.

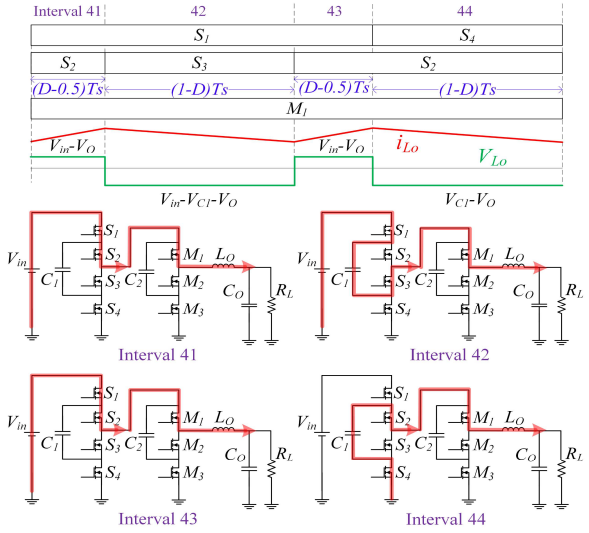


Fig. 5 Pulse arrangement, inductor current and voltage, and converter's equivalent circuit in Mode IV.

discharging C_1 and charging C_2. Therefore, the voltage across the inductor is equal to V_{C1}-V_{C2}-V_O, and the current variation is:

$$\Delta i_{Lo\_32} = \frac{(1-2D)T_S}{L_o}(V_{C1} - V_{C2} - V_O) \quad (12)$$

This interval finishes at t_{32}, when M_2 turns off and M_1 turns on.

Interval 33 [t_{32} t_{33}]: At t_{32}, M_1 turns on. S_2 and S_4 are still on from the previous interval. Therefore, the voltage across the inductor is equal to V_{C1} -V_O, and the inductor's current change is:

$$\Delta i_{Lo\_33} = \frac{(3D-1)T_S}{L_o}(V_{C1} - V_O) \quad (13)$$

This current discharges C_1. Interval 33 ends at t_{33}, when S_2 and S_4 turn off.

Interval 34 [t_{33} t_{34}]: At t_{33}, S_2 and S_4 turn off and M_1 stays on. Additionally, M_3 turns on. As a result, C_2 discharges and the inductor's current flows through M_1 and M_3 leading to V_{C2}-V_O across the inductor. So, its current variation is:

$$\Delta i_{Lo\_34} = \frac{(1-2D)T_S}{L_o}(V_{C2} - V_O) \quad (14)$$

This interval finishes at T_S, when M_3 turns off but M_1 stays on.

As the duty cycle moves from 1/3 to 1/2, intervals 2 and 4 lessen and finally become zero when $D=0.5$. At this condition, the voltage across the inductor is zero in all intervals, as a result the current ripple will be zero. As the duty cycle continues to increase beyond 0.5 up to 1 the converter enters Mode IV.

D. MODE IV: 1/2<D≤1

The pulse pattern and inductor's current in a switching cycle for the $1/2 \le D \le 1$, and the current flow in each interval, are presented in Fig. 5. Therefore, one switching cycle could be divided into four intervals that are explained in detail below.

Interval 41 [t_{40} t_{41}]: At t_{40}, S_1 and S_2 turn on. Since M_1 stays on throughout the switching cycle, the voltage across the inductor L_O becomes V_{in}-V_O. So, the inductor's current variation can be calculated as:

$$\Delta i_{Lo\_41} = \frac{(D-0.5)T_S}{L_o}(V_{in} - V_O) \quad (15)$$

This current flows through S_1, S_2 and M_1. The interval ends at t_{41}, when S_2 goes off.

Interval 42 [t_{41} t_{42}]: At t_{41}, S_2 goes off and S_3 turns on. Until t_{42}, S_1 and S_3 stay on. In this interval, the inductor's current flows through C_1 charging it. Therefore, the voltage across the inductor becomes V_{in}-V_{C1}-V_O, and the current variation is:

$$\Delta i_{Lo\_42} = \frac{(1-D)T_S}{L_o}(V_{in} - V_{C1} - V_O) \quad (16)$$

This interval finishes at t_{42}, when S_2 turns on while S_1 keeps staying on.

Interval 43 [t_{42} t_{43}]: At t_{42}, S_2 turns on and S_2 and M_1 are still on. So, in this interval, the voltage across the inductor becomes V_{in} -V_O, and the inductor's current change is:

$$\Delta i_{Lo\_43} = \frac{(D-0.5)T_S}{L_o}(V_{in} - V_O) \quad (17)$$

This current flows through S_1, S_2, and M_1, like interval 41. This interval ends at t_{43}, when S_1 turns off.

Interval 44 [t_{43} t_{44}]: At t_{43}, S_1, turns off while S_2 and M_1 continue to be on. At the same time S_4 also turns on. As a result, C_1 discharges and the inductor's current flows through M_1, S_2 and S_4 leading to V_{C1}-V_O across the inductor. So, its current variation is:

$$\Delta i_{Lo\_44} = \frac{(1-D)T_S}{L_o}(V_{C1} - V_O) \quad (18)$$

This interval finishes at T_S, when S_4 turns off but S_2 continues to stay on.

III. Theoretical Analysis of the Control Strategy

In this part, the output voltage, the flying capacitors' voltage, the inductor's current, and switches voltage stress equations are going to be derived for all four operation modes.

In Mode I, In the steady state the summation of inductor's current ripple is zero which is known as volt-second balance:

$$\Delta i_{Lo\_11} + \Delta i_{Lo\_12} + \Delta i_{Lo\_13} + \Delta i_{Lo\_14} + \Delta i_{Lo\_15} + \Delta i_{Lo\_16} = 0 \quad (19)$$

Therefore, substituting equations (1)-(6) into (19) computes the output voltage as:

$$V_O = DV_{in} \quad (20)$$

The initial value of inductor's current at the beginning of each switching cycle is defined as i_1, which is depicted in Fig. 6(a). Accordingly, the charge-second relation for C_1 using i_1 is:

$$DT_S\left(i_1 + \frac{\Delta i_{Lo\_11}}{2}\right) = DT_S\left(i_1 + \Delta i_{Lo\_11} + \Delta i_{Lo\_12} + \frac{\Delta i_{Lo\_13}}{2}\right) \quad (21)$$

The current waveform for this capacitor is depicted in Fig. 6(b), where its timing and current amplitudes are indicated. Using equations (1)-(3), and (20) in (21), gives:

$$V_{C12} = V_{in}/4 \quad (22)$$

where V_{C12} is the voltage of capacitor C_2 in Mode I.

In the same way, for the second flying capacitor the charge-second balance is:

$$DT_S\left(i_1 + \frac{\Delta i_{Lo\_11}}{2}\right) + DT_S\left(i_1 + \Delta i_{Lo\_11} + \Delta i_{Lo\_12} + \frac{\Delta i_{Lo\_13}}{2}\right) = 2DT_S\left(i_1 - \Delta i_{Lo\_16} - \frac{\Delta i_{Lo\_15}}{2}\right) \quad (23)$$

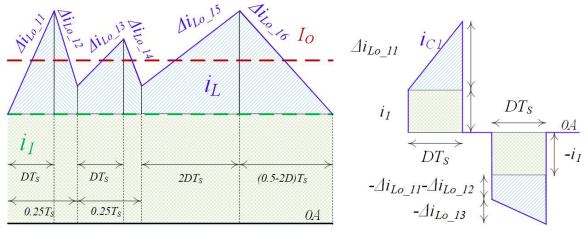
By substituting ripple current equations in equation (23) the first flying capacitors voltage can be written as:

$$V_{C11} = (D + 0.25)V_{in} \quad (24)$$

where V_{C11} is the voltage of capacitor C_1 in Mode I.

Now substitution of (20), (21), and (24) into (1), (3) and (5) gives:

$$\Delta i_{Lo\_11} = \frac{DT_S V_{in}}{L_o}(0.5 - 2D) \quad (25)$$



(a) (b)

Fig. 6 (a) Inductor current, and (b) the first flying capacitor current waveform for $0<D<1/4$

$$\Delta i_{Lo\_13} = \frac{DT_S V_{in}}{L_o}(D + 0.25 - 0.25 - D) = 0 \quad (26)$$

$$\Delta i_{Lo\_15} = \frac{2DT_S V_{in}}{L_o}(0.25 - D) \quad (27)$$

The above equations show that Δi_{Lo_13} is always zero when $0 \le D \le 1/4$, and when the duty cycle reaches 1/4, Δi_{Lo_11} and Δi_{Lo_15} also become zero. Moreover, at this moment ($D=1/4$) the time duration for the second, fourth, and sixth intervals goes down to zero making Δi_{Lo_12}, Δi_{Lo_14}, and Δi_{Lo_16}, equal to zero.

Hence, it can be concluded that the inductor current ripple at $D=1/4$ is zero.

In the same way, the flying capacitors' voltage and inductor's current in the other three modes can be calculated as:

Mode II:

$$V_{C21} = \frac{-8D^3+17D^2-8D+1}{14D^2-8D+1}V_{in} \quad (28)$$

$$V_{C22} = \frac{D^2(2D-1)}{14D^2-8D+1}V_{in} \quad (29)$$

$$\Delta i_{Lo\_21} = \frac{D(1-2D)(3D-1)(4D-1)T_s}{L_o(14D^2-8D+1)}V_{in} \quad (30)$$

$$\Delta i_{Lo\_22} = \frac{D(1-2D)(1-3D)(4D-1)T_s}{L_o(14D^2-8D+1)}V_{in} \quad (31)$$

$$\Delta i_{Lo\_23} = \frac{D(3D-1)(1-2D)(4D-1)T_s}{L_o(14D^2-8D+1)}V_{in} \quad (32)$$

$$\Delta i_{Lo\_24} = \frac{D(1-2D)(1-3D)(4D-1)T_s}{L_o(14D^2-8D+1)}V_{in} \quad (33)$$

The inductor's current ripple is zero at D=1/4 and 1/3.

Mode III:

$$V_{C31} = \frac{2D^2}{4D-1}V_{in} \quad (34)$$

$$V_{C32} = \frac{D^2}{4D-1}V_{in} \quad (35)$$

$$\Delta i_{Lo\_31} = \frac{D(2D-1)(3D-1)T_s}{L_o(1-4D)}V_{in} \quad (36)$$

$$\Delta i_{Lo\_32} = -\frac{(2D-1)(3D-1)T_s}{L_o(1-4D)}V_{in} \quad (37)$$

$$\Delta i_{Lo\_33} = \frac{(2D-1)(3D-1)T_s}{L_o(1-4D)}V_{in} \quad (38)$$

$$\Delta i_{Lo\_34} = -\frac{D(2D-1)(3D-1)T_s}{L_o(1-4D)} V_{in} \quad (39)$$

The inductor's current ripple is zero at *D=1/3* and *1/2*.

Mode IV:

$$V_{C41} = \frac{1}{2} V_{in} \quad (40)$$

$$\Delta i_{Lo\_41} = \frac{(2D-1)(1-D)T_s}{2L_o} V_{in} \quad (41)$$

$$\Delta i_{Lo\_42} = \frac{(2D-1)(D-1)T_s}{2L_o} V_{in} \quad (42)$$

The inductor's current ripple is zero at *D=1/2*.

The voltage conversion ratio of the converter with the new control method, in all four modes, is plotted in Fig. 7, which is the same as a conventional buck converter.

The other merit of the new control method is that the transition between the modes is smooth without any discontinuity or abrupt change in pulse pattern, voltage, or current. Fig. 8(a) shows the theoretical and experimental results for V_{Cf1} and V_{Cf2}, where verifies the continuous change of the voltages during all four modes and the transitions.

Based on the flying capacitors' voltage, the maximum voltage across the switches can be calculated in each mode. Fig. 8(b) shows the theoretical and experimental results for all seven switches in all four modes when V_O=*12V* and V_{in}=*20-60V*. Accordingly, the maximum voltage of the switches is always far below the input voltage. Therefore, low-voltage/low-cost switches can be utilized in this converter.

Fig. 9 compares the maximum current ripple of the inductor in the conventional and three-level buck converter and the ZIV converter with the proposed method The three-level buck and the proposed method have the same current ripple when *0.5≤D≤1*, because they operate the same. However, for *D≤0.5* the ZIV converter has significantly reduced the current ripple. Considering the input voltage range as V_{in}=*20-60V*, which is very common in many applications, the improvement becomes very notable.

IV. Experimental Results

The prototype specifications are listed in Table I. The output voltage is fixed at 12V, and the input voltage changes from 20V to 60V to cover all four modes. The experimental results at full load are presented in Fig. 10, for *D*=0.2, 0.25, 0.3, 0.33, 0.4, 0.5, and 0.6, to show the waveforms at all four modes as well as boundaries. In this figure, the gate pulse of switches S_1, S_2, and M_1 are shown along with the output inductor current (i_{Lo}), so it would be easier to compare the results with those explained in Fig. 2-5.

Fig. 10 (a), (c), (e), and (g) show the waveforms at modes I, II, III, and IV, respectively. In addition, the boundaries are shown in Fig. 10 (b), (d), and (f) for *D*=0.25, 0.33, and 0.5,

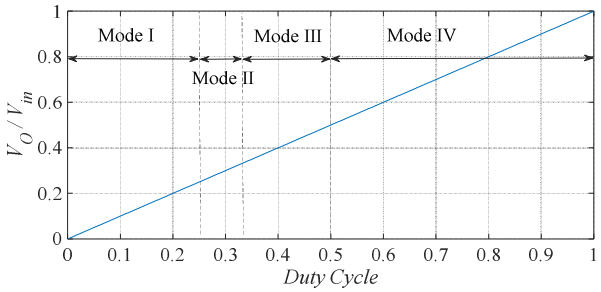
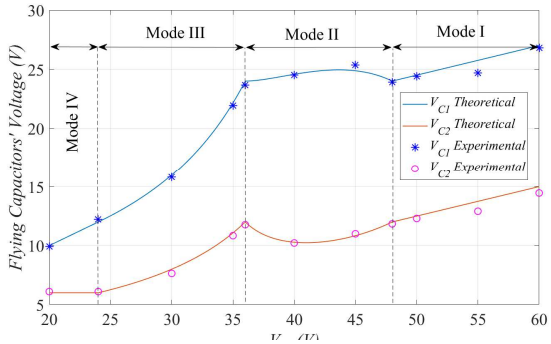
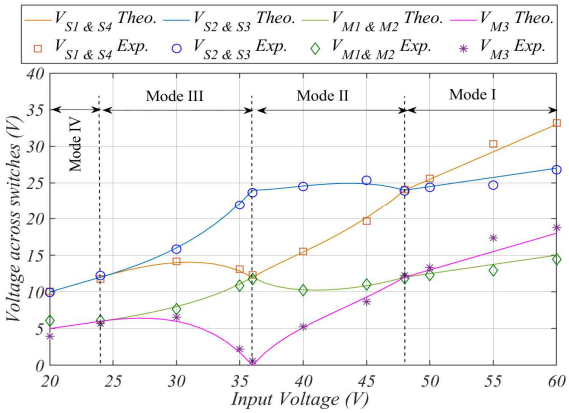


Fig. 7 Voltage conversion range of the converter versus duty cycle.



(a)



(b)

Fig. 8 Theoretical and Experimental results for (a) Flying capacitors' voltage, and (b) switches' voltage stress versus input voltage.

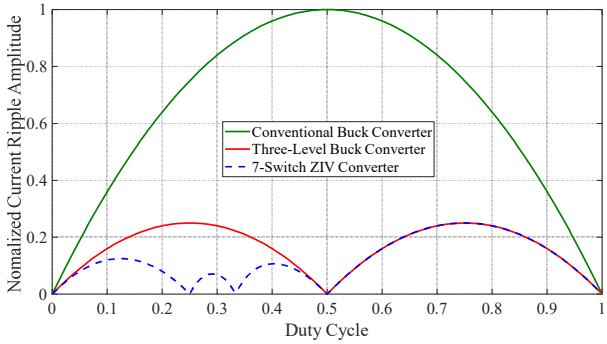


Fig. 9 Peak-to peak current ripple comparison among the 7-Switch, three-level, and conventional buck converters.

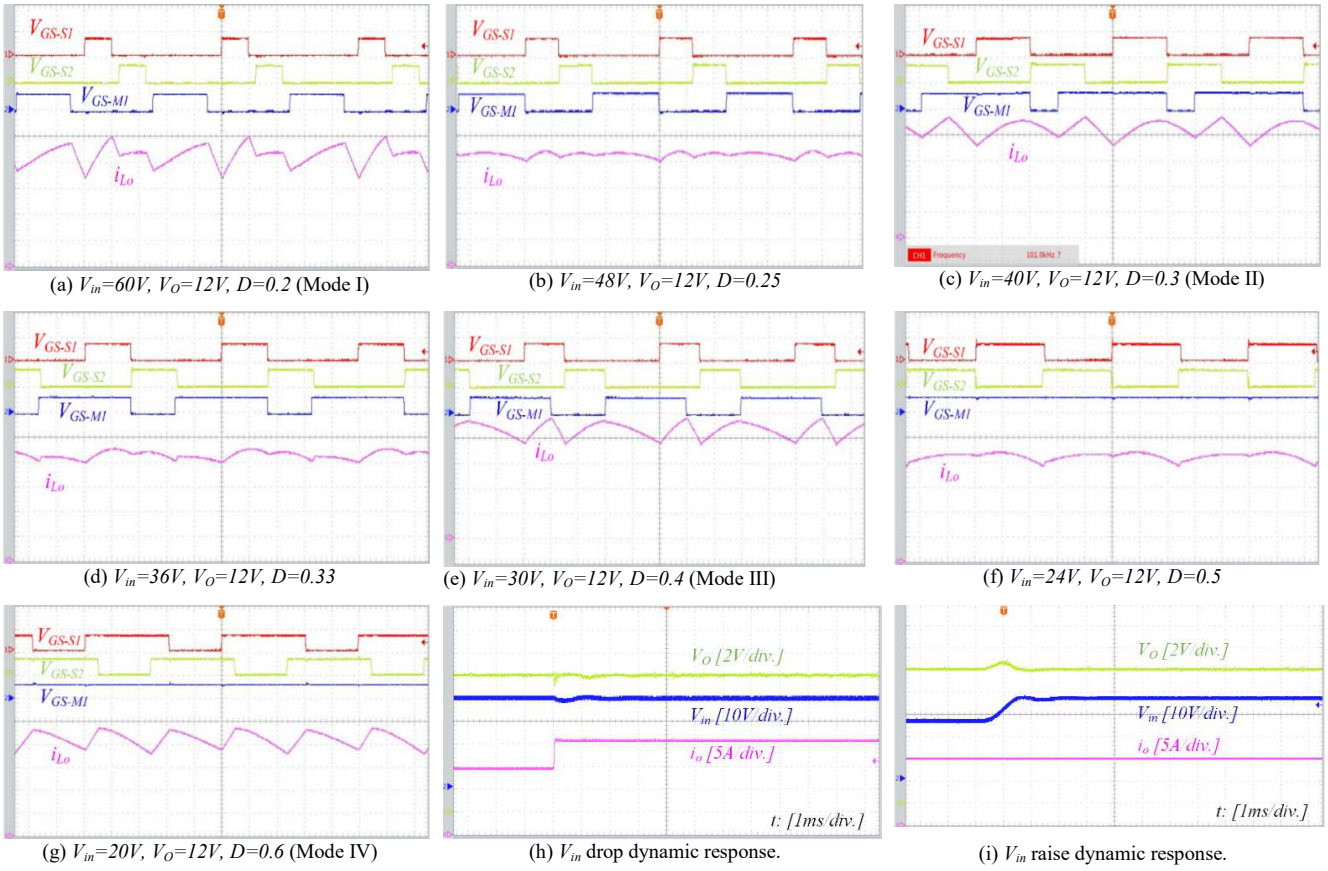
respectively. The capacitor's voltage ripple in conjunction with the switches deadtime causes the current waveform to become curvy in some intervals, especially at the boundary points. However, comparing these results with those presented in Fig. 2-5 reveals that the experimental results completely verify the theoretical analysis.

The converter's dynamic is shown in Fig. 10 (h) and (i). Fig. 10 (h) shows the proposed method response to I_O jump from 15A to 21A, where it shows that the converter has kept the output voltage finely at 12V. The line regulation response is shown in Fig. 10 (i), where the input voltage is jumped up from 27V to 37V, and the converter's operation is changed from Mode III to Mode II. Accordingly, the converter was able to keep the output voltage at 12V with a small overshoot in less than 2ms.

Fig. 11 shows the total efficiency (including control power loss). The average efficiency at full and light loads are 97.12% and 97.70%, respectively, and the peak efficiency is 98.5%. Also, the overall efficiency for the full range of the input voltage and output power is 97.54%. According to these figures, through the input voltage range the efficiency variations are small. From light load to full load, the average efficiency changes less than 0.6% which yields a good performance throughout the load and input voltage fluctuations.

TABLE I PROTOTYPE SPECIFICATION

Parameter	Value
V_{in}	20-60V
V_O	12V
P_O	250W
F_S	100kHz
C_{in}	7×10uF/100V
C_1	7×10uF/50V
C_2	7×10uF/50V
C_O	10×10uF/50V
L_O	2.2uH
S_1-S_4	BSZ025N04LS, 40V/2.5mΩ
M_1-M_3	SiSA04DN, 30V/2.15mΩ



(a) V_{in}=60V, V_O=12V, D=0.2 (Mode I)
(b) V_{in}=48V, V_O=12V, D=0.25
(c) V_{in}=40V, V_O=12V, D=0.3 (Mode II)
(d) V_{in}=36V, V_O=12V, D=0.33
(e) V_{in}=30V, V_O=12V, D=0.4 (Mode III)
(f) V_{in}=24V, V_O=12V, D=0.5
(g) V_{in}=20V, V_O=12V, D=0.6 (Mode IV)
(h) V_{in} drop dynamic response.
(i) V_{in} raise dynamic response.

Fig. 10 Experimental waveforms for (a)-(g) $V_{GS\text{-}S1}$[5V/div.], $V_{GS\text{-}S2}$[5V/div.], $V_{GS\text{-}M1}$[5V/div.], and i_{Lo} [5A/div.] at 250W output power and various duty cycles (t=2us/div.), (h)-(i) Dynamic response for input voltage step change.

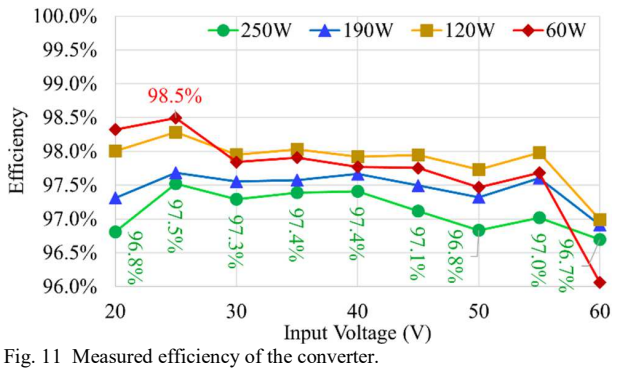


Fig. 11 Measured efficiency of the converter.

VI. Conclusion

A full-range voltage conversion (from zero to input voltage) technique for a step down 7-switch ZIV converter is introduced and analyzed in this paper without any additional component. The gate drive control strategy of the converter is divided into four different modes based on the required duty cycle value. As discussed in the paper, during the changeover between different modes, the transition is smooth and there is no discontinuity in the currents and voltages value. The other merit of this method is that it keeps the output inductor's current ripple small, in a way that the high efficiency of the ZIV converter is preserved. Also, with lower voltage across the inductor, smaller inductance is used which enhances the power density.

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